



## 4004 SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

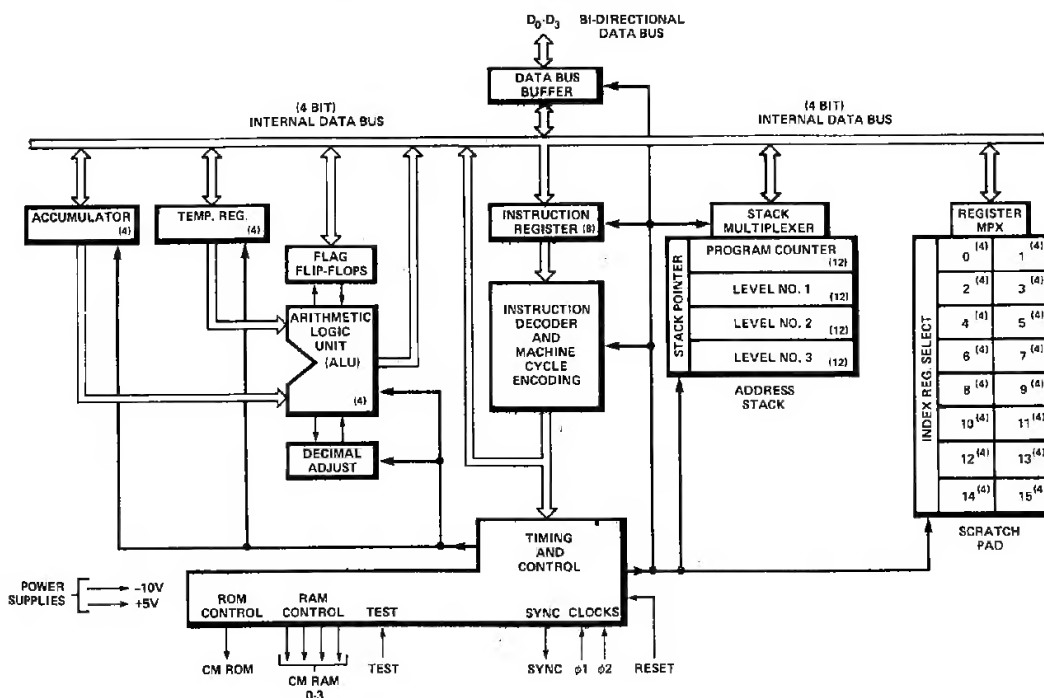
- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-40 ROMs and RAMs
- Easy Expansion — One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- Standard Operating Temperature Range of 0° to 70°C
- Also Available With -40° to +85°C Operating Range

The Intel® 4004 is a complete 4-bit parallel central processing unit (CPU). The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

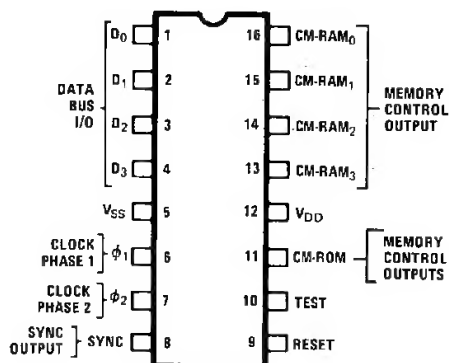
The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.

MCS 4/40



## Pin Description



### D<sub>0</sub>-D<sub>3</sub>

BIDIRECTIONAL DATA BUS. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

### RESET

RESET input. A logic "1" level at this input clears all flags and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 64 clock cycles (8 machine cycles).

### TEST

TEST input. The logical state of this signal may be tested with the JCN instruction.

### SYNC

SYNC output. Synchronization signal generated by the processor and set to the ROM and RAM chips. It indicates the beginning of an instruction cycle.

### CM-ROM

CM-ROM output. This is the ROM selection signal sent out by the processor when data is required from program memory.

### CM-RAM<sub>0</sub> – CM-RAM<sub>3</sub>

CM-RAM outputs. These are the bank selection signals for the 4002 RAM chips in the system.

### $\phi_1, \phi_2$

Two phase clock inputs.

### V<sub>SS</sub>

Most positive voltage.

### V<sub>DD</sub>

V<sub>SS</sub> -15 ±5% main supply voltage.



## Instruction Set Format

### A. Machine Instructions

- 1 word instruction — 8-bits requiring 8 clock periods (instruction cycle).
- 2 word instruction — 16-bits requiring 16 clock periods (2 instruction cycles).

Each instruction is divided into two four-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M<sub>1</sub> and M<sub>2</sub> times respectively.

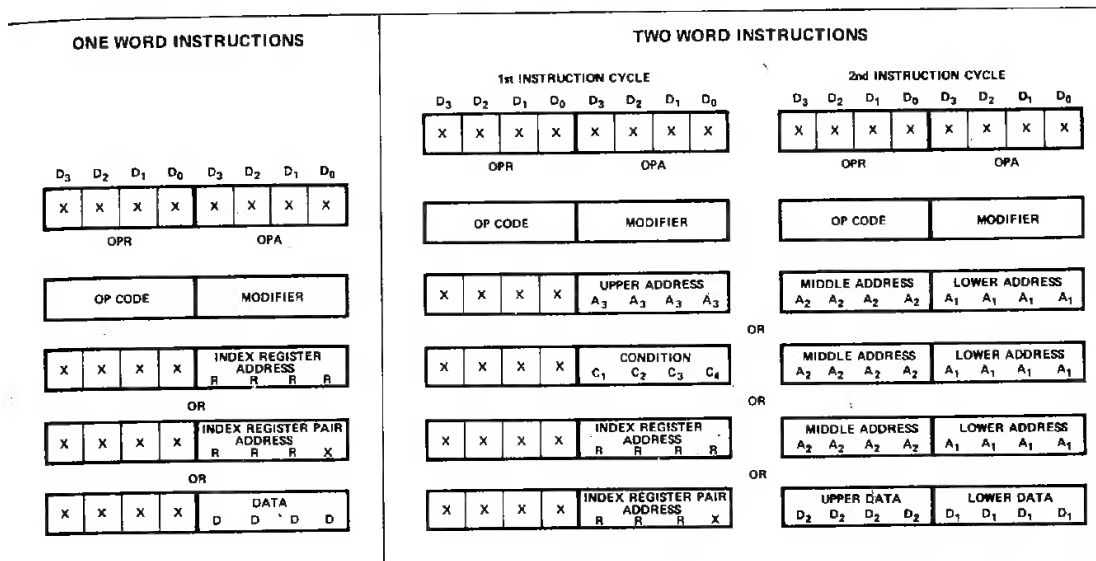


Table I. Machine Instruction Format

### B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

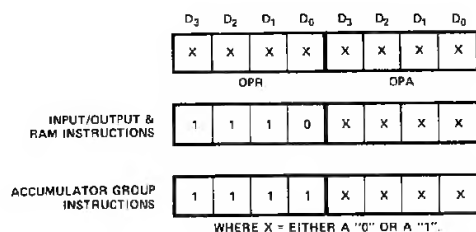


Table II. I/O and Accumulator Group Instruction Formats

## 4004 Instruction Set

## BASIC INSTRUCTIONS (\* = 2 Word Instructions)

| Hex Code  | MNEMONIC | OPR<br>D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>     | OPA<br>D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>   | DESCRIPTION OF OPERATION   |
|-----------|----------|--|--|--|
| 00        | NOP      | 0 0 0 0  | 0 0 0 0  | No operation.  |
| 1 -<br>-- | * JCN    | 0 0 0 1<br>A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> | C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> C <sub>4</sub><br>A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> | Jump to ROM address A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> , A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> (within the same ROM that contains this JCN instruction) if condition C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> C <sub>4</sub> is true, otherwise go to the next instruction in sequence. |
| 2 -<br>-- | * FIM    | 0 0 1 0<br>D <sub>2</sub> D <sub>2</sub> D <sub>2</sub> D <sub>2</sub> | R R R 0<br>D <sub>1</sub> D <sub>1</sub> D <sub>1</sub> D <sub>1</sub>   | Fetch immediate (direct) from ROM Data D <sub>2</sub> D <sub>2</sub> D <sub>2</sub> D <sub>2</sub> , D <sub>1</sub> D <sub>1</sub> D <sub>1</sub> D <sub>1</sub> to index register pair location RRR.  |
| 3 -       | FIN      | 0 0 1 1  | R R R 0  | Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.  |
| 3 -       | JIN      | 0 0 1 1  | R R R 1  | Jump indirect. Send contents of register pair RRR out as an address at A <sub>1</sub> and A <sub>2</sub> time in the instruction cycle.  |
| 4 -<br>-- | * JUN    | 0 1 0 0<br>A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> | A <sub>3</sub> A <sub>3</sub> A <sub>3</sub> A <sub>3</sub><br>A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> | Jump unconditional to ROM address A <sub>3</sub> A <sub>3</sub> A <sub>3</sub> A <sub>3</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> , A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> .  |
| 5 -<br>-- | * JMS    | 0 1 0 1<br>A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> | A <sub>3</sub> A <sub>3</sub> A <sub>3</sub> A <sub>3</sub><br>A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> | Jump to subroutine ROM address A <sub>3</sub> A <sub>3</sub> A <sub>3</sub> A <sub>3</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> , A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> , save old address (up 1 level in stack.)   |
| 6 -       | INC      | 0 1 1 0  | R R R R  | Increment contents of register RRRR.   |
| 7 -<br>-- | * ISZ    | 0 1 1 1<br>A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> | R R R R<br>A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> A <sub>1</sub>   | Increment contents of register RRRR. Go to ROM address A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> A <sub>2</sub> , A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> A <sub>1</sub> (within the same ROM that contains this ISZ instruction) if result ≠ 0, otherwise go to the next instruction in sequence.                                 |
| 8 -       | ADD      | 1 0 0 0  | R R R R  | Add contents of register RRRR to accumulator with carry.   |
| 9 -       | SUB      | 1 0 0 1  | R R R R  | Subtract contents of register RRRR to accumulator with borrow.   |
| A -       | LD       | 1 0 1 0  | R R R R  | Load contents of register RRRR to accumulator.   |
| B -       | XCH      | 1 0 1 1  | R R R R  | Exchange contents of index register RRRR and accumulator.  |
| C -       | BBL      | 1 1 0 0  | D D D D  | Branch back (down 1 level in stack) and load data DDDD to accumulator.   |
| D -       | LDM      | 1 1 0 1  | D D D D  | Load data DDDD to accumulator.   |
| F0        | CLB      | 1 1 1 1  | 0 0 0 0  | Clear both. (Accumulator and carry)  |
| F1        | CLC      | 1 1 1 1  | 0 0 0 1  | Clear carry.   |
| F2        | IAC      | 1 1 1 1  | 0 0 1 0  | Increment accumulator.   |
| F3        | CMC      | 1 1 1 1  | 0 0 1 1  | Complement carry.  |
| F4        | CMA      | 1 1 1 1  | 0 1 0 0  | Complement accumulator.  |
| F5        | RAL      | 1 1 1 1  | 0 1 0 1  | Rotate left. (Accumulator and carry)   |
| F6        | RAR      | 1 1 1 1  | 0 1 1 0  | Rotate right. (Accumulator and carry)  |
| F7        | TCC      | 1 1 1 1  | 0 1 1 1  | Transmit carry to accumulator and clear carry.   |
| F8        | DAC      | 1 1 1 1  | 1 0 0 0  | Decrement accumulator.   |
| F9        | TCS      | 1 1 1 1  | 1 0 0 1  | Transfer carry subtract and clear carry.   |
| FA        | STC      | 1 1 1 1  | 1 0 1 0  | Set carry.   |
| FB        | DAA      | 1 1 1 1  | 1 0 1 1  | Decimal adjust accumulator.  |
| FC        | KBP      | 1 1 1 1  | 1 1 0 0  | Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.   |
| FD        | DCL      | 1 1 1 1  | 1 1 0 1  | Designate command line.  |

**4001/4002/4008/4009/4289  
INPUT/OUTPUT AND RAM INSTRUCTIONS**

| Hex Code | MNEMONIC | OPR<br>D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub> | OPA<br>D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub> | DESCRIPTION OF OPERATION   |
|----------|----------|--|--|--|
| 2 -      | SRC      | 0 0 1 0  | R R R 1  | Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X <sub>2</sub> and X <sub>3</sub> time in the instruction cycle. |
| E0       | WRM      | 1 1 1 0  | 0 0 0 0  | Write the contents of the accumulator into the previously selected RAM main memory character.  |
| E1       | WMP      | 1 1 1 0  | 0 0 0 1  | Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)   |
| E2       | WRR      | 1 1 1 0  | 0 0 1 0  | Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)  |
| E3       | WPM      | 1 1 1 0  | 0 0 1 1  | Write the contents of the accumulator into the previously selected half byte of read/write program memory (used with 4008/4009 or 4289 only)                     |
| E4       | WR0      | 1 1 1 0  | 0 1 0 0  | Write the contents of the accumulator into the previously selected RAM status character 0.   |
| E5       | WR1      | 1 1 1 0  | 0 1 0 1  | Write the contents of the accumulator into the previously selected RAM status character 1.   |
| E6       | WR2      | 1 1 1 0  | 0 1 1 0  | Write the contents of the accumulator into the previously selected RAM status character 2.   |
| E7       | WR3      | 1 1 1 0  | 0 1 1 1  | Write the contents of the accumulator into the previously selected RAM status character 3.   |
| E8       | SBM      | 1 1 1 0  | 1 0 0 0  | Subtract the previously selected RAM main memory character from accumulator with borrow.   |
| E9       | RDM      | 1 1 1 0  | 1 0 0 1  | Read the previously selected RAM main memory character into the accumulator.   |
| EA       | RDR      | 1 1 1 0  | 1 0 1 0  | Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)  |
| EB       | ADM      | 1 1 1 0  | 1 0 1 1  | Add the previously selected RAM main memory character to accumulator with carry.   |
| EC       | RD0      | 1 1 1 0  | 1 1 0 0  | Read the previously selected RAM status character 0 into accumulator.  |
| ED       | RD1      | 1 1 1 0  | 1 1 0 1  | Read the previously selected RAM status character 1 into accumulator.  |
| EE       | RD2      | 1 1 1 0  | 1 1 1 0  | Read the previously selected RAM status character 2 into accumulator.  |
| EF       | RD3      | 1 1 1 0  | 1 1 1 1  | Read the previously selected RAM status character 3 into accumulator.  |



# 4004 Instruction Codes

| Hex | Mnemonic           | Hex | Mnemonic | Hex | Mnemonic | Hex | Mnemonic |
|-----|--------------------|-----|----------|-----|----------|-----|----------|
| 00  | —                  | 40  | JUN      | 80  | ADD 0    | C0  | BBL 0    |
| 01  | —                  | 41  | JUN      | 81  | ADD 1    | C1  | BBL 1    |
| 02  | —                  | 42  | JUN      | 82  | ADD 2    | C2  | BBL 2    |
| 03  | —                  | 43  | JUN      | 83  | ADD 3    | C3  | BBL 3    |
| 04  | —                  | 44  | JUN      | 84  | ADD 4    | C4  | BBL 4    |
| 05  | —                  | 45  | JUN      | 85  | ADD 5    | C5  | BBL 5    |
| 06  | —                  | 46  | JUN      | 86  | ADD 6    | C6  | BBL 6    |
| 07  | —                  | 47  | JUN      | 87  | ADD 7    | C7  | BBL 7    |
| 08  | —                  | 48  | JUN      | 88  | ADD 8    | C8  | BBL 8    |
| 09  | —                  | 49  | JUN      | 89  | ADD 9    | C9  | BBL 9    |
| 0A  | —                  | 4A  | JUN      | 8A  | ADD 10   | CA  | BBL 10   |
| 0B  | —                  | 4B  | JUN      | 8B  | ADD 11   | CB  | BBL 11   |
| 0C  | —                  | 4C  | JUN      | 8C  | ADD 12   | CC  | BBL 12   |
| 0D  | —                  | 4D  | JUN      | 8D  | ADD 13   | CD  | BBL 13   |
| 0E  | —                  | 4E  | JUN      | 8E  | ADD 14   | CE  | BBL 14   |
| 0F  | —                  | 4F  | JUN      | 8F  | ADD 15   | CF  | BBL 15   |
| 10  | JCN CN=0           | 50  | JMS      | 90  | SUB 0    | D0  | LDM 0    |
| 11  | JCN CN=1 also JNT  | 51  | JMS      | 91  | SUB 1    | D1  | LDM 1    |
| 12  | JCN CN=2 also JC   | 52  | JMS      | 92  | SUB 2    | D2  | LDM 2    |
| 13  | JCN CN=3           | 53  | JMS      | 93  | SUB 3    | D3  | LDM 3    |
| 14  | JCN CN=4 also JZ   | 54  | JMS      | 94  | SUB 4    | D4  | LDM 4    |
| 15  | JCN CN=5           | 55  | JMS      | 95  | SUB 5    | D5  | LDM 5    |
| 16  | JCN CN=6           | 56  | JMS      | 96  | SUB 6    | D6  | LDM 6    |
| 17  | JCN CN=7           | 57  | JMS      | 97  | SUB 7    | D7  | LDM 7    |
| 18  | JCN CN=8           | 58  | JMS      | 98  | SUB 8    | D8  | LDM 8    |
| 19  | JCN CN=9 also JT   | 59  | JMS      | 99  | SUB 9    | D9  | LDM 9    |
| 1A  | JCN CN=10 also JNC | 5A  | JMS      | 9A  | SUB 10   | DA  | LDM 10   |
| 1B  | JCN CN=11          | 5B  | JMS      | 9B  | SUB 11   | DB  | LDM 11   |
| 1C  | JCN CN=12 also JNZ | 5C  | JMS      | 9C  | SUB 12   | DC  | LDM 12   |
| 1D  | JCN CN=13          | 5D  | JMS      | 9D  | SUB 13   | DD  | LDM 13   |
| 1E  | JCN CN=14          | 5E  | JMS      | 9E  | SUB 14   | DE  | LDM 14   |
| 1F  | JCN CN=15          | 5F  | JMS      | 9F  | SUB 15   | DF  | LDM 15   |
| 20  | FIM 0              | 60  | INC 0    | A0  | LD 0     | E0  | WRM      |
| 21  | SRC 0              | 61  | INC 1    | A1  | LD 1     | E1  | WMP      |
| 22  | FIM 2              | 62  | INC 2    | A2  | LD 2     | E2  | WRR      |
| 23  | SRC 2              | 63  | INC 3    | A3  | LD 3     | E3  | WPM      |
| 24  | FIM 4              | 64  | INC 4    | A4  | LD 4     | E4  | WRO      |
| 25  | SRC 4              | 65  | INC 5    | A5  | LD 5     | E5  | WR1      |
| 26  | FIM 6              | 66  | INC 6    | A6  | LD 6     | E6  | WR2      |
| 27  | SRC 6              | 67  | INC 7    | A7  | LD 7     | E7  | WR3      |
| 28  | FIM 8              | 68  | INC 8    | A8  | LD 8     | E8  | SBM      |
| 29  | SRC 8              | 69  | INC 9    | A9  | LD 9     | E9  | RDM      |
| 2A  | FIM 10             | 6A  | INC 10   | AA  | LD 10    | EA  | RDR      |
| 2B  | SRC 10             | 6B  | INC 11   | AB  | LD 11    | EB  | ADM      |
| 2C  | FIM 12             | 6C  | INC 12   | AC  | LD 12    | EC  | RDO      |
| 2D  | SRC 12             | 6D  | INC 13   | AD  | LD 13    | ED  | RD1      |
| 2E  | FIM 14             | 6E  | INC 14   | AE  | LD 14    | EE  | RD2      |
| 2F  | SRC 14             | 6F  | INC 15   | AF  | LD 15    | EF  | RD3      |
| 30  | FIN 0              | 70  | ISZ 0    | B0  | XCH 0    | F0  | CLB      |
| 31  | JIN 0              | 71  | ISZ 1    | B1  | XCH 1    | F1  | CLC      |
| 32  | FIN 2              | 72  | ISZ 2    | B2  | XCH 2    | F2  | IAC      |
| 33  | JIN 2              | 73  | ISZ 3    | B3  | XCH 3    | F3  | CMC      |
| 34  | FIN 4              | 74  | ISZ 4    | B4  | XCH 4    | F4  | CMA      |
| 35  | JIN 4              | 75  | ISZ 5    | B5  | XCH 5    | F5  | RAL      |
| 36  | FIN 6              | 76  | ISZ 6    | B6  | XCH 6    | F6  | RAR      |
| 37  | JIN 6              | 77  | ISZ 7    | B7  | XCH 7    | F7  | TCC      |
| 38  | FIN 8              | 78  | ISZ 8    | B8  | XCH 8    | F8  | DAC      |
| 39  | JIN 8              | 79  | ISZ 9    | B9  | XCH 9    | F9  | TCS      |
| 3A  | FIN 10             | 7A  | ISZ 10   | BA  | XCH 10   | FA  | STC      |
| 3B  | JIN 10             | 7B  | ISZ 11   | BB  | XCH 11   | FB  | DAA      |
| 3C  | FIN 12             | 7C  | ISZ 12   | BC  | XCH 12   | FC  | KBP      |
| 3D  | JIN 12             | 7D  | ISZ 13   | BD  | XCH 13   | FD  | DCL      |
| 3E  | FIN 14             | 7E  | ISZ 14   | BE  | XCH 14   | FE  | —        |
| 3F  | JIN 14             | 7F  | ISZ 15   | BF  | XCH 15   | FF  | —        |

## Absolute Maximum Ratings\*

|   |                  |
|---|------------------|
| Ambient Temperature Under Bias                                    | 0°C to 70°C      |
| Storage Temperature   | -55°C to + 125°C |
| Input Voltages and Supply Voltage with respect to V <sub>SS</sub> | +0.5V to -20V    |
| Power Dissipation   | 1.0 Watt         |

**\*COMMENT:**  
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## D.C. and Operating Characteristics

T<sub>A</sub> = 0°C to 70°C; V<sub>SS</sub> - V<sub>DD</sub> = 15V ± 5%; t<sub>φPW</sub> = t<sub>φD1</sub> = 400 nsec; logic "0" is defined as the more positive voltage (V<sub>IH</sub>, V<sub>OH</sub>); logic "1" is defined as the more negative voltage (V<sub>IL</sub>, V<sub>OL</sub>); Unless Otherwise Specified.

### SUPPLY CURRENT

| Symbol          | Parameter              | Min. | Limit Typ. | Max. | Unit | Test Conditions       |
|-----------------|------------------------|------|------------|------|------|-----------------------|
| I <sub>DD</sub> | Average Supply Current |      | 30         | 40   | mA   | T <sub>A</sub> = 25°C |

### INPUT CHARACTERISTICS

|                  |                                    |                      |  |                       |    |                                   |
|------------------|------------------------------------|----------------------|--|-----------------------|----|-----------------------------------|
| I <sub>LI</sub>  | Input Leakage Current              |                      |  | 10                    | μA | V <sub>IL</sub> = V <sub>DD</sub> |
| V <sub>IH</sub>  | Input High Voltage (Except Clocks) | V <sub>SS</sub> -1.5 |  | V <sub>SS</sub> +3    | V  |                                   |
| V <sub>IL</sub>  | Input Low Voltage (Except Clocks)  | V <sub>DD</sub>      |  | V <sub>SS</sub> -5.5  | V  |                                   |
| V <sub>ILO</sub> | Input Low Voltage                  | V <sub>DD</sub>      |  | V <sub>SS</sub> -4.2  | V  | 4004 TEST Input                   |
| V <sub>IHC</sub> | Input High Voltage Clocks          | V <sub>SS</sub> -1.5 |  | V <sub>SS</sub> +3    | V  |                                   |
| V <sub>ILC</sub> | Input Low Voltage Clocks           | V <sub>DD</sub>      |  | V <sub>SS</sub> -13.4 | V  |                                   |

### OUTPUT CHARACTERISTICS

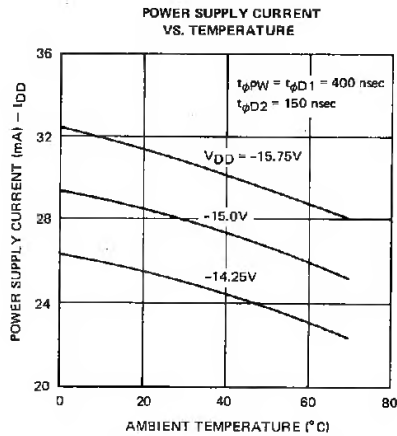
|                 |   |                     |                 |                      |    |   |
|-----------------|---|---------------------|-----------------|----------------------|----|---|
| I <sub>LO</sub> | Data Bus Output Leakage Current               |                     |                 | 10                   | μA | V <sub>OUT</sub> = -12V                 |
| V <sub>OH</sub> | Output High Voltage                           | V <sub>SS</sub> -5V | V <sub>SS</sub> |                      | V  | Capacitance Load                        |
| I <sub>OL</sub> | Data Lines Sinking Current                    | 8                   | 15              |                      | mA | V <sub>OUT</sub> = V <sub>SS</sub>      |
| I <sub>OL</sub> | CM-ROM Sinking Current                        | 6.5                 | 12              |                      | mA | V <sub>OUT</sub> = V <sub>SS</sub>      |
| I <sub>OL</sub> | CM-RAM Sinking Current                        | 2.5                 | 6               |                      | mA | V <sub>OUT</sub> = V <sub>SS</sub>      |
| V <sub>OL</sub> | Output Low Voltage, Data Bus, CM, SYNC        | V <sub>SS</sub> -12 |                 | V <sub>SS</sub> -6.5 | V  | I <sub>OL</sub> = 0.5mA                 |
| R <sub>OH</sub> | Output Resistance, Data Line "0" Level        |                     | 150             | 250                  | Ω  | V <sub>OUT</sub> = V <sub>SS</sub> -.5V |
| R <sub>OH</sub> | CM-ROM Output Resistance, Data Line "0" Level |                     | 320             | 600                  | Ω  | V <sub>OUT</sub> = V <sub>SS</sub> -.5V |
| R <sub>OH</sub> | CM-RAM Output Resistance, Data Line "0" Level |                     | 1.1             | 1.8                  | kΩ | V <sub>OUT</sub> = V <sub>SS</sub> -.5V |

### CAPACITANCE

|                  |                      |  |    |    |    |                                   |
|------------------|----------------------|--|----|----|----|-----------------------------------|
| C <sub>φ</sub>   | Clock Capacitance    |  | 14 | 20 | pF | V <sub>IN</sub> = V <sub>SS</sub> |
| C <sub>DB</sub>  | Data Bus Capacitance |  | 7  | 10 | pF | V <sub>IN</sub> = V <sub>SS</sub> |
| C <sub>IN</sub>  | Input Capacitance    |  |    | 10 | pF | V <sub>IN</sub> = V <sub>SS</sub> |
| C <sub>OUT</sub> | Output Capacitance   |  |    | 10 | pF | V <sub>IN</sub> = V <sub>SS</sub> |

## 4004

### Typical D.C. Characteristics



### A.C. Characteristics

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{SS} - V_{DD} = 15V \pm 5\%$

| Symbol         | Parameter   | Min. | Limit<br>Typ. | Max. | Unit            | Test Conditions                 |
|----------------|---|------|---------------|------|-----------------|---------------------------------|
| $t_{CY}$       | Clock Period  | 1.35 |               | 2.0  | $\mu\text{sec}$ |                                 |
| $t_{\phi R}$   | Clock Rise Time   |      |               | 50   | ns              |                                 |
| $t_{\phi F}$   | Clock Fall Times  |      |               | 50   | ns              |                                 |
| $t_{\phi PW}$  | Clock Width   | 380  |               | 480  | ns              |                                 |
| $t_{\phi D1}$  | Clock Delay $\phi_1$ to $\phi_2$                                      | 400  |               | 550  | ns              |                                 |
| $t_{\phi D2}$  | Clock Delay $\phi_2$ to $\phi_1$                                      | 150  |               |      | ns              |                                 |
| $t_W$          | Data-In, CM, SYNC Write Time  | 350  | 100           |      | ns              |                                 |
| $t_H^{[1,3]}$  | Data-In, CM, SYNC Hold Time   | 40   | 20            |      | ns              |                                 |
| $t_H^{[3]}$    | Data Bus Hold Time During $M_2$ - $X_1$ and $X_2$ - $X_3$ Transition. | 150  |               |      | ns              |                                 |
| $t_{OS}^{[2]}$ | Set Time (Reference)  | 0    |               |      | ns              |                                 |
| $t_{ACC}$      | Data-Out Access Time  |      |               |      |                 | $C_{OUT} =$                     |
|                | Data Lines  |      |               | 930  | ns              | 500pF Data Lines                |
|                | Data Lines  |      |               | 700  | ns              | 200pF Data Lines <sup>[4]</sup> |
|                | SYNC  |      |               | 930  | ns              | 500pF SYNC                      |
|                | CM-ROM  |      |               | 930  | ns              | 160pF CM-ROM                    |
|                | CM-RAM  |      |               | 930  | ns              | 50pF CM-RAM                     |
| $t_{OH}$       | Data-Out Hold Time  | 50   | 150           |      | ns              | $C_{OUT} = 20pF$                |

Notes: 1.  $t_H$  measured with  $t_{\phi R} = 10\text{nsec}$ .

2.  $T_{ACC}$  is Data Bus, SYNC and CM-line output access time referred to the  $\phi_2$  trailing edge which clocks these lines out.  $t_{OS}$  is the same output access time referred to the leading edge of the next  $\phi_2$  clock pulse.

3. All MCS-40 components which may transmit instruction or data to the 4004 at  $M_2$  and  $X_2$  always enter a float state until the 4004 takes over the data bus at  $X_1$  and  $X_3$  time. Therefore the  $t_H$  requirement is always insured since each component contributes  $10\mu\text{A}$  of leakage current and  $10pF$  of capacitance which guarantees that the data bus cannot change faster than  $1V/\mu\text{s}$ .

4.  $C_{DATA BUS} = 200pF$  if 4008 and 4009 or 4289 is used.



The timing diagram illustrates the relationship between various signals and clock phases. The horizontal axis represents time, divided into segments by vertical lines. The signals shown are:

- X<sub>3</sub>**: Address bus signal, active during the first and last segments.
- A<sub>1</sub>**: Address bus signal, active during the first segment.
- A<sub>2</sub>**: Address bus signal, active during the second segment.
- A<sub>3</sub>**: Address bus signal, active during the third segment.
- M<sub>1</sub>**: Memory strobe, active during the fourth segment.
- M<sub>2</sub>**: Memory strobe, active during the fifth segment.
- X<sub>1</sub>**: Address bus signal, active during the sixth segment.
- X<sub>2</sub>**: Address bus signal, active during the seventh segment.
- X<sub>3</sub>**: Address bus signal, active during the eighth segment.
- DATA BUS**: Data bus signal, active during the first, second, third, fourth, fifth, sixth, seventh, and eighth segments.
- φ<sub>1</sub>**: Clock phase 1, a square wave signal.
- φ<sub>2</sub>**: Clock phase 2, a square wave signal.
- SYNCH**: Synchronization signal, active during the first, second, third, fourth, fifth, sixth, seventh, and eighth segments.
- CM RAM, ROM**: Chip select signal, active during the first, second, third, fourth, fifth, sixth, seventh, and eighth segments.

Additional labels and annotations include:

- CPU ENABLED**: Label for the first, second, third, fourth, fifth, sixth, seventh, and eighth segments.
- ROM ENABLED**: Label for the fourth and fifth segments.
- OPA (4004) AC (4040) CPU ENABLED**: Label for the sixth segment.
- IF IOR ELSE CPU ENABLED**: Label for the seventh segment.
- IF I/O**: Label for the sixth segment.
- IF SRC**: Label for the seventh segment.
- 10%**: Annotation for the first and eighth segments.
- 90% 90%**: Annotation for the seventh segment.

Figure 1. Schematic representation of the experimental design. The subjects were divided into two groups: the control group (n = 10) and the experimental group (n = 10). The control group received a standard diet (SD) and the experimental group received a high-fat diet (HFD). The subjects were divided into two groups: the control group (n = 10) and the experimental group (n = 10). The control group received a standard diet (SD) and the experimental group received a high-fat diet (HFD). The subjects were divided into two groups: the control group (n = 10) and the experimental group (n = 10). The control group received a standard diet (SD) and the experimental group received a high-fat diet (HFD).

